REMARKS

The present amendment is prepared in accordance with the new revised requirements of 37 C.F.R. § 1.121. A complete listing of all the claims in the application is shown above showing the status of each claim. For current amendments, inserted material is underlined and deleted material has a line therethrough.

Applicants appreciate the thoroughness with which the Examiner has examined the above-identified application. Reconsideration is requested in view of the amendments above and the remarks below.

Claims 1-6, 14, 19 and 20 have been amended.

Claims 11 and 12 have been canceled.

Claims 21 and 22 have been added.

No new matter has been added.

Claim Rejections – 35 USC § 103

The Examiner has rejected claims 1-12, 19 and 20 under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. (U.S. Patent No. 6,333,563) in view of Kobayashi (U.S. Patent No. 6,806,560). Applicants disagree.

Jackson is directed to increasing the fatigue life of a BGA within an electrical interconnection package. (Abstract.) It discloses a chip 10 secured to a substrate 20 using at least one solder ball 12 and an underfill material 14 between the chip and substrate. (Col. 2, ll. 53-63 and Fig. 1.) A first set of single melt solder alloy material interconnects 22 are joined between the substrate 20 and organic interposer 30. An underfill 24 of a low melt material fills the exposed area between the substrate 20 and the interposer 30. (Col. 3, ll. 6-41, and Fig. 2.) A second set of interconnect materials

32 having a higher melting temperature are attached to the bottom side of the organic interposer 30 to establish a temperature hierarchy between the higher melting interconnect materials 32 and the low melting underfill material 24. (Col. 3, ll. 25-41.) The interposer is then joined to an organic board 40 using the dual melt material 32. (Col. 3, ll. 42-57 and Fig. 4.)

By underfilling the first set of single melt solder alloy material interconnects 22 within this low melting underfill material 24, a key aspect of Jackson is that the interconnects 22 will not melt either when the higher melting interconnect materials 32 are joined to the interposer 30, or when the interposer 30 is joined to the board 40. (Col. 3, ll. 35-41 and col. 4, ll. 7-21.)

Jackson does not disclose or suggest providing an underfill material in the space between the circuit board and the substrate, nor does it disclose the cleaning step. The Examiner acknowledges this deficiency of Jackson in the above-identified office action.

To overcome these deficiencies, the Examiner cites Kobayashi stating that it discloses an underfill material 32 injected into a space between a chip mounting substrate and a printed circuit board 30 to enhance the adhesive strength there-between (citing, Abstract and Figs. 1 and 2D).

It is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the method of Jackson et al. by depositing further an underfill material in the space between the circuit board, since the underfill material is capable of adsorbing stresses due to TCE between the chip-mounting substrate and the board, thereby securing the soldered joint and further enhance the adhesive strength between the chip-mounting substrate and the board (Kobayashi: abstract, and column 1, lines 34-41).

Applicants disagree.

Applicants submit that Kobayashi discloses a chip 20 adhered to a central area of a chip mounting substrate 10 comprising a single layer substrate 11 with through holes 12, lands 13, wiring pads 14 connected to the lands 13 via the through holes 12, solder balls 24 on the wiring pads 14, and a solder mask 15 with unevenness on a bottom surface thereof. (Col. 6, ll. 32-55 and Fig. 2D.) A board 30 with pads 31 connected to solder balls 24 is connected to the chip-mounting substrate 10 at the Cu wiring pads 14. Unevenness is provided on a bottom surface of a solder mask 15 of the chip mounting substrate 10 and then this bottom surface of the chip mounting substrate 10 is washed. (Col. 7, ll. 17-21.) The chip mounting substrate 10 is then attached to the board, and then underfill material 32 is injected into a clearance between the chip mounting substrate 10 and the board 30. (Col. 7, ll. 22-37 and Fig. 2D.)

With respect to claims 1 and 19, applicants submit that these claims are directed to a method for assembling an electronic module, and an electronic module assembly, that include a chip attached to a substrate using a first solder interconnection array and a board attached to the substrate using a second solder interconnection array to define a space there-between. This space between the substrate and the board has a gap height ranging from about 300 microns to about 900 microns. A rigid matrix of an underfill material is provided within this space and in contact with the board and the substrate, prior to applying any compressive forces to the electronic module, for maintaining this space and optimizing integrity of the second solder interconnection array during application of compressive forces. This underfill material has a filler material with a particle size ranging from about 32 microns to about 300 microns present in an amount ranging from about 60 to 64 weight percent.

It is submitted that the combination of Jackson and Kobayashi does not disclose or suggest an underfill material of having such particle sizes and weight percents between a substrate and a board. Moreover, these references, either alone or in combination, do not disclose or suggest also having a mechanical support structure within the space between the substrate and the board (in addition to the underfill material), whereby this mechanical support structure may be a rigid metallic ball (claims 2 and 20), a bracket (claims 3 and 20), a frame (claims 4 and 20), or even a collar (claim 20). Jackson in view of Kobayashi also does not disclose or contemplate only partially underfilling this space to partially encapsulate the second solder interconnection array at discrete locations only (new claims 21 and 22). Accordingly, these claims are not obvious over the cited references.

Similarly, claim 5 is directed to a method for assembling an electronic module that includes attaching a chip to a substrate using a first solder interconnection array, and attaching an organic board to the substrate using a second solder interconnection array to define a space there-between. An underfill material is deposited at discrete locations within this space for partially encapsulating the second solder interconnection array at these discrete locations. The underfill is then cured to form a rigid matrix within the space to maintain and enhance integrity of the second solder interconnection array.

Applicants submit that neither Jackson nor Kobayashi, alone or in combination, disclose or contemplate providing an underfill material in a space between a substrate and a board only at discrete locations within this space. Rather, the cited references are limited to completely underfilling spaces. As such, Jackson and Kobayashi, alone or in combination, do not disclose or contemplate the combinations of a partial underfill

between a substrate and a board in combination with the limitations of cleaning and heating the board prior to underfill deposition (claim 6), the addition of a rigid metallic ball (claim 7) or other mechanical support structures (claim 8), or even that the second solder interconnection is a single melt solder (claim 9) or a dual melt solder (claim 10).

The Examiner has also rejected claims 14-18 under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. (U.S. Patent No. 6,333,563)in view of Kobayashi (U.S. Patent No. 6,806,560) as applied to claim 5 above, and further in view of Kumamoto et al. (U.S. Patent No. 6,632,704).

The Examiner recognizes that neither Jackson et al. or Kobayashi expressly teach the properties of the underfill material including density, particle size viscosity dynamic tensile modulus as set forth in claims 14-18. To overcome this deficiency the Examiner cites Kumamoto et al. stating that it discloses the properties of a desirable epoxy underfill material applied in a surface-mount processing of an electronic device for the purpose of relieving significant portions of thermal loads induced by CTE differences between a chip and a substrate (column 1, line 55 – column 2, line 1).

Applicants disagree.

Kobayashi is limited to disclosing epoxies for filling a gap between a chip and a substrate, which is not what the invention is directed towards. As recognized by the Examiner, Kobayashi discloses an underfill material having a filler material present in an amount ranging from about 80% by weight per solution, with the filler material having a particle size ranging from about 4μ - 12μ (i.e., 4-12 microns). Applicants' specification recites that these conventional underfill materials having filler particle sizes ranging from about 1 micron to about 25 microns in diameter are commonly used to underfill the smaller gap dimensions, and are inadequate as underfill materials for

the present larger interconnection grid arrays since they precipitously flow-out from these larger interconnection grid arrays, and thereby leave gaps or voids within such interconnection grid arrays such that the interconnection grid arrays are not entirely encapsulated. (Specification, paragraph [0063].)

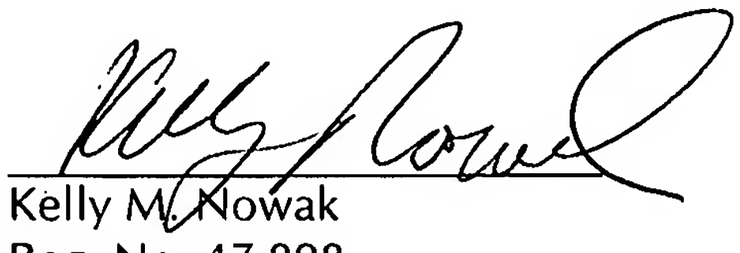
The present invention discloses an underfill material having material present in an amount ranging from about 60% by weight per solution to about 64% by weight per solution, and having a particle size ranging from about 32 microns to about 300 microns in diameter. It is submitted that this is a difference in kind, not degree, such that Kobayashi does not rectify the deficiencies of Jackson or Kobayashi, alone or in combination.

Applicants submit that the suggestion to make the claimed structure, carry out the claimed process and the reasonable expectation of success there-from must be founded in the prior art, not in Applicant's disclosure. *In re Vaech* (CAFC 1991) 20 USPQ2d 1438. The cited reference, and not in retrospect, must suggest doing what Applicants have done. *In re Skoll* (CCPA 1975) 187 USPQ 481. Applicants submit that the cited references, alone or in combination, do not suggest doing what applicants have done, such that applicants' invention would only be found based on applicants' own disclosure, which of course is improper as a hindsight reconstruction of applicants' invention. *Id., W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983) (Hindsight based on reading of the patent in issue may not be used to aid in determining obviousness). Likewise, hindsight and the level of ordinary skill in the art may not be used to supply a component missing from the cited references. *Al-Site Corp. v. VSI International, Inc.*, 174 F.3d 1308, 1324, 50 USPQ2d 1161, 1171 (Fed. Cir. 1999).

In view of the foregoing, and under the applicable patent law in this area, it is respectfully submitted that the claims are properly allowable under 35 USC 103.

It is respectfully submitted that the application has now been brought into a condition where allowance of the case is proper. Reconsideration and issuance of a Notice of Allowance are respectfully solicited. Should the Examiner not find the claims to be allowable, Applicants' attorney respectfully requests that the Examiner call the undersigned to clarify any issue and/or to place the case in condition for allowance.

Respectfully submitted,



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